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		STATE	MENT UNDER 37 CFF	R 3.73(b)	2047.0600003
Applicant/Patent Owner: Garg et al.					
Application	No./Patent No.:	5,838,986	Filed/Issue Date:	November 1	17, 1998
RISC Microprocessor Architecture Implementing Multiple Typed Register Sets					
(Name of Assig	Transmeta Corp	oration	, a(Type of Assignee, e.g.	corporation ., corporation, partnershi	ip, university, government agency, etc.)
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1. F	rom:	Garg et al.	To: Inited States Patent and T	S-MOS Sys	stems, Inc.
Reel <u>014201</u> , Frame <u>0448</u> , or for which a copy thereof is attached.					
2. F			To:To:		
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X Additional documents in the chain of title are listed on a supplemental sheet.					
X As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11. [NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]					
The undersigned (whose title is supplied to by) is authorized to act on behalf of the assignee. Signature Date					
	Donald J. Fe	eatherstone, Reg	g. No. 33,876		(202) 371-2600
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	Att	orney for Paten	tees		
		Title			

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